Office Action Summary	Application No.	Applicant(s)	
	10/822,275	JANZEN, JEFFERY W.	
	Examiner	Art Unit	
	CRAIG E. WALTER	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Interview Summary

1. Ms. Karen Lenaburg (Reg. No. 58,371) contacted Examiner on 11 June 2008 to request withdrawing the finality of the previously issued Office action (mailed 19 March 2008). The details of that conversation are captured in the attached PTO-413 form.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 22 January 2008 has been entered.

Status of Claims

3. Claims 1-30 are pending in the Application.

Claims 1, 10, 21 and 26 are amended.

Claims 1-30 are rejected.

Response to Amendment

4. Applicant's amendments and arguments filed on 22 January in response to the office action mailed on 20 November 2007 have been fully considered, but they are not

persuasive. Therefore, the rejections made in the previous office action are maintained, and restated below, with changes as needed to address the amendments.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 8 and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 8 and 19 recite the limitation "the data bus" in line 2 of the claim. There is insufficient antecedent basis for this limitation in the claim, as a plurality of data busses are previously set forth in these claims (i.e. each memory device includes a data bus). Which bus is being referenced by the phrase “the bus” in these claims?

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ryan (US PG Publication 2004/0044833 A1), in further view of Schumacher et al. (US Patent 5,502,621), hereinafter Schumacher.

As for claims 1, 10, 21, and 26, Ryan teaches a memory module comprising:

a data input device (Fig. 3 (311));

a data output device (Fig. 3 (312));

a processor coupled to the data input and data output devices (Fig. 3 (304));

memory modules comprising:

a circuit board (Fig. 3 (201));

a plurality of memory devices positioned around a memory hub (Fig. 3 (memory devices (212, 214, …); hub (208))) on the same side of a circuit board; and

an edge connector positioned along an edge of the circuit board (paragraph 0006, all lines – Ryan discusses DIMM devices which contain edge connectors – see also claim 12 of Ryan).

Ryan additionally teaches coupling data signals between the memory hub and each memory device (this is inherent for data to be written into, and read from, each memory device), and a plurality of command-address busses, wherein each command-address bus coupled to the memory hub and at least two memory devices, the two memory devices being from a different pair (Ryan discloses at least one “vertical bus” (e.g. elements 230, 232, 238 and 240), and at least one “horizontal bus” (e.g. elements 234, 236, 242 and 244)).

Despite these teachings Ryan fails to teach each memory device being positioned in a pairs, in which the paired devices are arranged such that each respective device has the same pinout, yet one is rotated 180 degrees with respect to the board such that first and second sets of functional pins are adjacent (and substantially abutting) to each other.

Schumacher however teaches arranging ICs in a paired configuration such that one device is rotated 180 degrees with respect to the board – Fig. 4, devices 410 and 415 are ICs with the same pinout, just mirrored with respect to the vertical axis (i.e. 180 degree rotation). Schumacher teaches this configuration in order to keep similar functional pin groupings together (col. 3, lines 40-56). Note Schumacher teaches pairs of ICs that substantially abut each other (see Fig. 4).

Schmacher additionally teaches each respective memory device without pins or lead extending beyond an outer perimeter as described in the claim ("an outer perimeter of each respective device" is in fact the terminating end of the leads of Schumacher's memory device. As such, Schumacher teaches memory devices, "without pins or lead extending beyond an outer perimeter of each memory device).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Ryan to further include Schumacher's system of mirrored pin assignment for two sided multi-chip layout into his own system and method for optimizing interconnections of memory devices in a multichip module. By doing so, Ryan would be able to connect the memory devices of his memory system with a more simplified lead

routing scheme, which in turn would lead to a reduction of the number of layers in the PCB as taught by Schumacher in col. 2 lines 35-39.

As for claims 3, 12, and 22, Ryan teaches the memory module of claim 1 wherein the memory devices comprise DRAMs (paragraph 0004, all lines).

As for claim 23, Ryan teaches the computer system of claim 21 wherein the memory modules are coupled in a daisy chain manner to the controller (referring to Fig. 4, each memory module (201, 302) is connected to the controller (not shown in this figure, but shown in Fig. 2 (200), in a daisy chained fashion via a connecting bus (401))).

As for claim 24, Ryan teaches the computer system of claim 21 wherein the high-speed data link comprises an optical communications link (paragraph 0019, all lines).

As for claim 29, Ryan teaches the method of claim 26 wherein a data bus is routed between the hub and each device, and wherein signal lines of the data bus are routed substantially parallel edges of the circuit board (referring to Fig. 2, each bus (230, 232) is routed parallel with the edges of the board).

As for claim 30, the Ryan discloses the method of claim 26 wherein a control-address bus is routed between the hub and one device in each pair (Fig. 2, each bus is routed to one device. The bus contains control and data signals), and wherein signal lines of the control-address bus as being routed diagonally outward from the hub towards corners of the circuit board (though Ryan does not explicitly teach signal lines of the control-address bus are routed diagonally outward from the hub towards corners of the circuit board, such a limitation is merely a matter of design choice and would have

been obvious in the system of Ryan. The mere routing of the signal lines (either orthogonally, or diagonally) fails to define a patentably distinct invention over Ryan since both the instant invention as a whole, and Ryan's teachings are directed to optimizing the connections in multi-chip modules).

As for claims 4 and 13, Ryan teaches a DIMM device (which contains connectors on the edges of both sides of the board – paragraph 0006, all lines and claim 12 of Ryan).

As for claims 7, 9, 18, 20 and 25, Ryan teaches module includes eight pairs of memory devices, they fail to teach four pairs positioned on a front side of the circuit board and four pairs positioned on a back side of the circuit board, each pair on the front side being positioned adjacent a corresponding pair on the back side, and wherein the eight pairs of memory devices comprise a single rank on the memory module (Ryan discloses a DIMM device with varying number of chips – paragraph 0006, all lines and claim 12 of Ryan. A DIMM device by definition contains memory devices on both sides of a PCB).

As for claims 8 and 19, though Ryan in fact teaches a memory bus which is 64 bits wide (paragraph 0008, all lines)), he fails to specifically teach a bus with half of them as 4-bits wide, and the remaining half 5-bits wide as recited in these claims. It would however have been obvious to one of ordinary skill in the art for Ryan to use a bus for his memory containing more or less than 64 bits (i.e. half of them with a 4-bit wide bus, and half with a 5-bit bus). Ryan's system would benefit using a smaller bus width bits by increasing the aerial density of his PCB, since less trace lines would be

required to transfer data between the memory and the hub. The limitation of using a 4-bit or 5-bit wide memory bus (rather than 64 as expressly taught by Ryan) fails to define a patentably distinct invention over Ryan, since both the instant invention as a whole and Ryan's teachings are directed to optimizing the connections in multi-chip modules.

As for claims 6 and 15, though Ryan fails to specifically teach a memory bus as being 9-bits wide (he in fact teaches a memory bus, which is 64 bits wide (paragraph 0008, all lines)), it would have been obvious to one of ordinary skill in the art for Ryan to use a bus for his memory containing more or less than 64 bits. Ryan's system would benefit using a smaller bus width bits by increasing the aerial density of his PCB, since less trace lines would be required to transfer data between the memory and the hub. The limitation of using an 18-bit wide memory bus (rather than 64 as expressly taught by Ryan) fails to define a patentably distinct invention over Ryan, since both the instant invention as a whole and Ryan's teachings are directed to optimizing the connections of multi-chip modules.

As for claim 16, Ryan teaches his modules includes a first pair of memory devices positioned adjacent a respective edge of the circuit board and a second pair positioned adjacent an diagonal opposite edge of the circuit board (Fig. 2., each memory pair (i.e. 212, 214) is arranged adjacent a pair located on a second edge of the board (i.e. 222, 220). Note, Though Ryan does not explicitly teach pairs of memory devices as being opposite on a diagonal from each other (rather they are opposite with respect to a horizontal and/or vertical axis), such a limitation is merely a matter of design choice and would have been obvious in the system of Ryan. The mere

positioning of opposite pairs (either being opposites with respect to a horizontal or diagonal axis of the board) fails to define a patentably distinct invention over Ryan since both the instant invention as a whole and Ryan's teachings are directed to optimizing the connections of multi-chip modules.

As for claim 17, though Ryan teaches his memory bus as being 64-bits wide rather than 18-bits as claimed by Applicant, (paragraph 0008, all lines), it would have been obvious to one of ordinary skill in the art for Ryan to use a bus for his memory containing more or less than 64 bits (i.e. 18 bits). Ryan's system would benefit using a smaller bus width bits by increasing the aerial density of his PCB, since less trace lines would be required to transfer data between the memory and the hub. The limitation of using an 18-bit wide memory bus (rather than 64 as expressly taught by Ryan) fails to define a patentably distinct invention over Ryan, since both the instant invention as a whole and Ryan's teachings are directed to optimizing the connections of multi-chip modules.

As for claims 2 and 11, Schumacher teaches a memory module wherein the first functional group of signals comprise data signals and the second functional group of signals comprise control-address signals (col. 3, lines 40-56).

As for claims 5, and 14, Ryan teaches the modules as including devices, each pair being positioned substantially perpendicular to adjacent pairs and located adjacent to a respective edge of the circuit board (see Fig. 3 – note though 8 devices are shown, the number could be more or less per paragraph 0021, final 11 lines of this paragraph). Also note Ryan teaches pairs and being perpendicular with respect to each other (Fig.

2, memory pairs are located at 90 degree angles with respect to each of the four side). Despite these teachings, he fails however to teach the devices as being arranged in pairs, such that the first functional group of signals comprising data signals and the second functional group of signals comprising control-address signals. Schumacher however teaches this very configuration (as per the rejection of claims 1 and 2).

As for claim 27, Schumacher teaches the method of claim 26 wherein each memory device includes a pin 1 designated end and a first functional group of signals are adjacent this end of the device, and wherein the devices in each pair are positioned with the pin 1 designated ends substantially abut one another (just as stated above for the rejection of claim 2, the memory devices are arranged to keep similar functional pins together – col. 3, lines 40-56).

As for claim 28, Schumacher teaches the method of claim 27 wherein the first functional group of signals comprises data bus signals (as per the rejection of claim 2).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Ryan to further include Schumacher's system of mirrored pin assignment for two sided multi-chip layout into his own system and method for optimizing interconnections of memory devices in a multichip module. By doing so, Ryan would be able to connect the memory devices of his memory system with a more simplified lead routing scheme, which in turn would lead to a reduction of the number of layers in the PCB as taught by Schumacher in col. 2 lines 35-39.

Double Patenting

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

8. A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

9. Claims 1-30 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 37 of copending Application No. 11/417,389 (hereinafter Application '379) in view of Ryan (US PG Publication 2004/0044833 A1), and in further view of Schumacher (US Patent 5,502,621). The minor differences between claim 21 (selected as representative of the remaining base claims of the instant application as it is the most comprehensive of the set) of the instant application and claim 37 of the co-pending application are presented in the matrix below.

Instant Application 10/822,275	Co-pending Application 11/417,389
Claim 21:	Claim 37:
A computer system, comprising: a data input device;	A memory module, comprising:
a data output device;	
a processor coupled to the data input and data output devices;	
a controller electrically coupled to the processor, the controller being operable to receive and transmit memory signals on a high-speed data link;	
at lease one memory module coupled to the controller, each memory module comprising:	
a circuit board;	a circuit board;
a memory hub positioned on the circuit board;	a memory controller positioned on the circuit board;
a plurality of pairs of memory devices positioned around the memory hub and arranged in pairs on the same side of the circuit board as one another,	a plurality of memory devices positioned around the memory hub and arranged in pairs,
each memory device having the same physical layout including pins associated with a first functional group of signals adjacent a first end of each memory device and pins associated with a second functional group of signals adjacent a second end of each memory device, and the first end of each device in each pair being positioned substantially abutting one another on the circuit board;	each memory device having a first edge and a second opposite the first edge and further having a same arrangement of electrical terminals relative to the first and second edges, including a first group of electrical terminals to which first-type signals are coupled and a second group of electrical terminals to which second-type signals are coupled, the first group of electrical terminals positioned adjacent the first edge and the second group of electrical terminals positioned adjacent the second edge, the second edge of each device in a pair positioned adjacent a second edge of a memory device in one of the other pairs
and an *edge* connector *positioned along an edge of the circuit board* and coupled to the memory hub.	a connector coupled to the memory hub and configured to couple at least one of command, address, and data signals to the memory hub

Note Ryan teaches several of the elements that claim 37 of Application '379 lacks, including:

a data input device (Fig. 3 (311));

a data output device (Fig. 3 (312));

a processor coupled to the data input and data output devices (Fig. 3 (304));

a controller electrically coupled to the processor, the controller being operable to receive and transmit memory signals on a high-speed data link (paragraph 0019, all lines);

a memory hub positioned on the circuit board (Fig. 3 element 208);

memory devices on the same side of a circuit board (again, Fig. 3); and

an edge connector positioned along the edge of the circuit board (memory modules are described as being DIMM devices – paragraph 0006, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Application '379 to further include Ryan's system and method for optimizing interconnections of memory devices in a multichip module into his own system for mirroring memory devices. By doing so, Application '379 would be able to exploit the timing benefits of Ryan's system including minimizing skew, and maximizing signal integrity between the hub and memory devices by positioning them equidistant from a centralized hub as taught by Ryan in paragraphs 0012 through 0013, all lines.

Despite these teachings Ryan fails to teach each memory device being positioned in a pairs, in which the paired devices are arranged such that each respective device has the same pinout, yet one is rotated 180 degrees with respect to the board such that first and second sets of functional pins are substantially abutting each other.

Schumacher however teaches arranging ICs in a paired configuration such that one device is rotated 180 degrees with respect to the board – Fig. 4, devices 410 and 415 are ICs with the same pinout, just mirrored with respect to the vertical axis (i.e. 180 degree rotation). Schumacher teaches this configuration (i.e. chips substantially abutting one another) in order to keep similar functional pin groupings together (col. 3, lines 40-56).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Application '379 to further include Schumacher's system of mirrored pin assignment for two sided multi-chip layout into his own system for mirroring memory devices. By doing so, Application '379 would be able to connect the memory devices of the memory system with a more simplified lead routing scheme, which in turn would lead to a reduction of the number of layers in the PCB as taught by Schumacher in col. 2 lines 35-39.

10. The remaining claims 1-20 and 22-30 are further rejected as being obvious over claim 37 of Application '379 in further view of Ryan (US PG Publication 2004/0044833 A1) in further view of Schumacher (US Patent 5,502,621). The minor differences between the copending claims and the pending claims of the instant application are

rendered obvious in view of the combined teachings of Ryan and Schumacher based on the rationale set forth under the art rejections of these claims as discussed supra. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Response to Arguments

11. As for claims 8 and 19 (with respect to the § 112(2) rejections), Applicant failed to address the previous rejections either in argument or by way of amendment; therefore these rejections are maintained and restated above.

12. Applicant's arguments with respect to rejections set forth under obviousness-type double patenting and 35 USC § 103(a) have been considered but they are not persuasive.

Applicant's arguments are predicated on an interpretation of Ryan, wherein each element described as a means for communicating commands and addresses (e.g. elements 230, 240, etc.) is in of itself, a unique bus. Likewise, the argument that Schmacher fails to teach memory devices without pins or lead extending beyond an outer perimeter of each memory device, is predicated on an assumption is that the "outer perimeter" of the memory devices does not includes the leads themselves.

These arguments however are not persuasive. With respect to the former, Examiner maintains that in one particular embodiment, Ryan discloses at least one "vertical bus" (e.g. elements 230, 232, 238 and 240), and at least one "horizontal bus" (e.g. elements 234, 236, 242 and 244). Based on this interpretation, Ryan clearly

teaches "each command-address bus [as being] coupled to the memory hub and at least two memory devices, the two memory devices being from a different pair", Applicant's arguments notwithstanding.

With respect to the latter, Examiner maintains "an outer perimeter of each respective device" is in fact the terminating end of the leads of Schumacher's memory device. As such, Schumacher teaches memory devices, "without pins or lead extending beyond an outer perimeter of each memory device", Applicant's arguments notwithstanding.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to CRAIG E. WALTER whose telephone number is (571)272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

14. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

15. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Craig E Walter/
Patent Examiner, Art Unit 2188

CEW